REMARKS

Claims 1-14 are pending. Claims 1-5, 7-12, and 14 have been amended. No new matter is believed to be added by these amendments.

I. Amendments

Claims 1-5, 7-12, and 14 have been amended to clarify "queue set" to read "queue set data structure." Support for this amendment can be found at least in Figure 1, and page 4, paragraph 19 of the present application.

Claims 1 and 8 have been further amended to state: "transforming a plurality of consecutive packets into a queue set data structure based on a target queue set data structure size." Support for this amendment can be found at least on page 7, paragraph 29 and page 10, paragraph 35 of the present application.

Claims 2 and 9 have been further amended to state:

> determining a size of each of the plurality of consecutive packets; and
>
> allocating the plurality of consecutive packets to the queue set data structure based on a target queue set data structure size according to the consecutive packet sizes, the target queue set data structure size being approximate to a largest supported packet length of the queue.

Support for this amendment can be found on page 10, paragraph 37 of the present application.

II. 35 U.S.C. §102b Rejections

Claims 1-14 are currently pending in the present application. Of these pending claims, claims 1 and 8 are independent claims. Claims 2-7 and 9-14 depend therefrom. In the Office Action, claims 1, 5, and 6 were rejected under 35 U.S.C. §102(b) as unpatentable over United States Patent. No. 5,463,620 (hereinafter "*Sriram*").

A proper rejection of a claim under 35 U.S.C. §102 requires that a single prior art reference disclose each element of the claim. *See, e.g., W.L. Gore & Assoc., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303, 313 (Fed. Cir. 1983). The 35 U.S.C. §102 test is the same for a process. Anticipation requires identity between the claimed process and a process of the prior art. The claimed process, including each step thereof, must have been described or embodied, either expressly or inherently, in a single reference. *See, e.g., Glaverbel S.A. v. Northlake Mkt'g & Supp., Inc.,* 45 F.3d 1550, 33 USPQ2d 1496 (Fed. Cir. 1995). Those elements must either be inherent or disclosed expressly. *See, e.g., Constant v. Advanced Micro-Devices, Inc.,* 848 F.2d 1560, 7 USPQ2d 1057 (Fed. Cir. 1988); *Verdegaal Bros., Inc. v. Union Oil Co.,* 814 F.2d 628, 2 USPQ2d 1051 (Fed. Cir. 1987). For anticipation, there must be no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention. *See, e.g., Scripps Clinic & Res. Found. v. Genentech, Inc.,* 927 F.2d 1565, 18 USPQ2d 1001 (Fed. Cir. 1991). In summary, the single prior art reference must properly disclose, teach or suggest each element of the claimed invention. Moreover, "every element of the claimed invention must be literally present, arranged as in the claim. … The identical invention must be shown in as complete detail as is contained in the patent claim." *See, e.g., Richardson v. Suzuki Motor Company Co.,* 868 F.2d 1226, 1236 (Fed. Cir. 1989).

Sriram does not anticipate claim for at least the reason that all the claim limitations have not been met. *Sriram* does not teach at least the limitations of "**transforming** a plurality of consecutive packets into a **queue set data structure based on a target queue set data**

structure size" or "performing a queuing operation on the queue set data structure, the queuing operation **treating the queue set data structure as a single entity**" as recited in claim 1.

Sriram is directed toward Asynchronous Transfer Mode (ATM) networks that utilize fixed sized "cells." *Sriram* teaches, in column 3, lines 43-55, that "traffic through each of the nodes is classified in accordance with certain signal characteristics" and then there "is at least one queue in the queuing mechanism for each traffic classification." Finally, a "server multiplexes the contents of the queuing mechanism" into an output link. *Sriram* discusses various types of traffic that the system will encounter from column 3, line 61 to column 4, line 63. The types of traffic are divided based on bandwidth and delivery requirements. *Sriram* discloses his invention in Figure 5 and its concordant description. At column 5, lines 7-11, Sriram states that, "communications traffic is classified in accordance with certain signal characteristics" and "is selectively directed to a number of different queuing circuits based upon the results of the classification." Then, at column 5, lines 35-39,

> dynamic time slice (DTS) server defines a predetermined cycle time D_c during which it visits each of the queuing circuits in sequence and withdraws a predetermined number of ATM cells from the queuing circuit withdraws a predetermined number of ATM cells from the queuing circuit and transfers that predetermined number of cells onto the output link.

In essence, *Sriram* sorts incoming cells based on data type, then inserts the cells into a queue circuit. Importantly, the cells are individually placed in the queue, as is known in the art. The cells are not placed into a data structure remotely analogous to a "queue set data structure" as required by claim 1. Furthermore, the cells are individually placed in the queue without regard to "a target queue set data structure size" as required by claim 1. *Sriram* simply individually inserts the cells into a queue individually. At a certain time, as taught in column 5, lines 56

through column 6, line 2, the DTS server of *Sriram* withdraws a plurality of cells from a queue and transmits the plurality of cells in order to guarantee an agreed upon amount of service for each class of cells. However, this withdraw of a group of cells is in no way analogous to "treating the queue set data structure as a single entity" as is recited in claim 1. The cells of *Sriram* that are withdrawn were not transformed into a single data structure. Accordingly, the cells of *Sriram* that are withdrawn are merely the next predetermined number of individually queued cells. This aspect of pulling cells from the queue is scheduling, the cells are not placed into the queue as a single entity. One skilled in the art would not look to scheduling algorithms to solve problems related to queuing.

Since *Sriram* does not teach all the claim limitations, *Sriram* cannot render the present claims unpatentable. Accordingly, Applicants respectfully request withdrawal of this rejection, and allowance of claims 1-14. Since the Applicants respectfully assert that independent claim 1 is allowable, dependent claims 2-7 are also allowable.

III. 35 U.S.C. §103(a)

Claims 1-14 are currently pending in the present application. Of these pending claims, claims 1 and 8 are independent claims. Claims 2-7 and 9-14 depend therefrom. In the Office Action, claims 2-4 and 7-14 were rejected under 35 U.S.C. §103(a) as unpatentable over *Sriram* in view of a number of other patent and patent publication references.

Applicants first submit that, for a *prima facie* case of obviousness, the cited prior art references (when combined) "must teach or suggest all the claim limitations" MPEP § 2143. Thus, if the combination of references does not teach each of the claimed limitations, a finding of obviousness fails. In addition, the Patent Office has the burden under § 103 to establish a *prima facie* case of obviousness, which can be satisfied only by showing some objective teaching

in the prior art would lead one to combine the relevant teachings of the references. *See In re Fine*, 837 F.2d 1071, 1074 (Fed. Cir. 1988). As such, an Applicant, to overcome an allegation of obviousness can show that the cited prior art references (when combined) do not teach or suggest all the claim limitations or that there is not an objective teaching in the prior art that would lead one to combine the relevant teachings of the references.

The Office Action, on page 9, item 12, rejected claim 8 under 35 U.S.C. §103(a) as unpatentable over *Sriram* in view of United States Patent. No. 5,926,458 (hereinafter "*Yin*"). However, *Sriram* in view of *Yin* does not render claim 8 obvious for at least the reason that all the claim limitations have not been met. Regarding claim 8, as discussed above with regard to a similar rejection of claim 1 under 35 U.S.C. §102(a) rejection over *Sriram*, *Sriram* does not teach the limitations of "a queue set data structure generator configured for **transforming** a plurality of consecutive packets **into a queue set data structure based on a target queue set data structure size**" or a "scheduler configured for performing a queuing operation on the queue set data structure, the queuing operation **treating the queue set data structure as a single entity**" as recited in claim 8. *Yin* does not correct these failings of *Sriram*. At column 4, lines 41-51, *Yin* merely teaches a communication link that provides "queue status information from queues 46-52 to packet scheduler 28."

Furthermore, the combination of *Sriram* and *Yin* would not have been made by one of skill in the art. *Sriram* deals with placing ATM cells into various queues based on cell type, and then a DTS server withdraws cells from each queue on a timed basis. There is no need in *Sriram* to provide a notification to the DTS server of the status of any of the queues. At column 4, lines 41-51, *Yin* teaches that "queue status information transmitted on communication link 56 may

include the size of the packet at the head of each queue (i.e., the next packet in the queue to be transmitted), and information indicating whether a particular queue is full or empty." As described in column 6, lines 20-44, the DTS server of *Sriram* has a cyclical method of checking queues that is integral to operation of the system. The DTS server has no need to know the status of the queues. As stated in *Sriram*,

> The server 48 in effect defines a cycle time period D_c during which it will retrieve cells from all of the queues having cells to send. The server 48 divides the cycle time period into time slices T_1, T_2, . . . T_n, assigns a time slice to each of the queues, and permits each queue to empty cells onto the output link 28 during its respective time slice. The server 48 accomplishes this by visiting each queue in sequence, removing a predetermined number of cells from each queue, and then moving on to remove a predetermined number of cells from the next queue in sequence. All queues are visited within the next cycle time period D_c defined by the server 48. At the completion of the cycle time period, the server 48 repeats the cycle of visiting each queue and removing respective predetermined numbers of cells from each queue within the cycle time period. If any one of the queues contains no cells, then the server completely passes over the empty queue and immediately moves on to the next queue in sequence to remove its allotted number of cells. If any of the queues contains a number of cells which is less than the predetermined number of cells the server 48 is scheduled to remove during a cycle time period, then the server 48 removes cells from that queue until it is empty and immediately moves on to the next queue to remove its allotted number of cells. Thus, the server 48 may complete a cycle of removing cells from all queues in an amount of time which is less than the cycle time period.

To provide the DTS server of *Sriram* with the communication link of *Yin* would be inefficient and possibly disrupt the purpose of the ATM queuing system taught by *Sriram*. In sum, to combine the two references would not only **not** produce the presently claimed invention, but would produce a system for transmitting ATM cells and providing unnecessary information to

the DTS server. Applicants earnestly request reconsideration, withdrawal of this rejection, and allowance of claims 1-14. Since the Applicants respectfully assert that independent claim 8 is allowable, dependent claims 9-14 are also allowable.

Additionally, the Office Action, on page 4, rejected claim 2 under 35 U.S.C. §103(a) as unpatentable over *Sriram* in view of United States Patent Application Publication No. 2001/0007565 (hereinafter "*Weng*"). Applicants address this rejection as analogous limitations are now found in both independent claims 1 and 8. *Weng* does not teach "allocating the plurality of consecutive packets to the queue set based on a target queue set size, the target queue set size being approximate to a largest supported packet length of the queue" as originally claimed in claim 2, before this amendment. Neither does *Weng* teach the current limitation of claim 2, "allocating the plurality of consecutive packets to the queue set data structure based on a target queue set data structure size according to the consecutive packet sizes, the target queue set data structure size being approximate to a largest supported packet length of the queue". Finally, *Weng* does not teach the limitation of "transforming a plurality of consecutive packets into a queue set data structure based on a target queue set data structure size" found in both independent claims 1 and 8, as amended.

Weng teaches, in paragraph 35, that "packet buffers 220a, 220b, 220c in the storage unit 220 are each sized fixedly to the maximum allowable packet length specified by the network protocol." This is merely describing allocating a buffer size according to a maximum packet length available to a protocol. This does not teach transforming packets for transmission as a single entity based on a target size. Modifying buffer size based on maximum packet length is not analogous to having a single data structure that represents a plurality of packets, wherein the single data structure has a target size. As disclosed in the present application on page 11,

paragraph 37, "[d]ue to the variability in the length of packets, a packet can be stored in a queue et whose size makes the queue set greater than the target queue size (e.g. 2048 bytes) across all queue sets." The application plainly states that target queue size is not necessarily linked to the maximum packet length of a protocol. Nowhere in *Weng* is taught a single data structure that represents a plurality of packets, wherein the single data structure was constructed based on a target size.

Furthermore, the combination of *Sriram* and *Weng* would not have been made by one of skill in the art. *Sriram* deals with ATM networks and cells of fixed size. There are no packets of variable length in *Sriram*, much less a need for a buffer size to support the largest packet length. To combine the two references would not only **not** produce the presently claimed invention, but would produce a system for transmitting ATM cells through a buffer fixed at 53 octets. Furthermore, one skilled in the art would not look to teachings related to buffering to address problems with queuing/scheduling. Applicants earnestly request reconsideration, withdrawal of this rejection, and allowance of claims 1-14.

Second, the Supreme Court has reaffirmed the *Graham* factors for determination of obvious under 35 U.S.C. 103(a). *KSR Int'l Co. v. Teleflex, Inc.* (*KSR*), No 04-1350 (U.S. Apr. 30, 2007). The four factual inquiries under *Graham* require examination of: (1) the scope and contents of the prior art; (2) the differences between the prior art and the claims in issue; (3) the level of ordinary skill in the pertinent art; and (4) the objective evidence of secondary consideration. *Graham v. John Deere* (*Graham*), 383 U.S. 1, 17-18, 149 USPQ 459, 467 (1966); see also 35 U.S.C. § 103 (2000).

The Court has further recognized that the requirement for a teaching, suggestion or

motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings, which was established by the Court of Customs and Patent Appeals, provides a helpful insight for determining whether the claimed subject matter is obvious under 35 U.S.C. § 103(a). In addition, the Court maintained that any analysis supporting a rejection under 35 U.S.C. § 103(a) should be made explicit, and that it is "important to identify reasons that would have prompted a person of ordinary skill in the relevant field to combine the [prior art] elements" in the manner claimed, because "inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known." *KSR* at 14, 15.

Where an invention is contended to be obvious based upon a combination of elements across different references, one should be able to identify particular reasons that would have prompted a person of ordinary skill in the relevant field to combine the [prior art] elements. *See, KSR Int'l Co.*, at 14, 15. This requirement prevents the use of "the inventor's disclosure as a blueprint for piecing together the prior art to defeat patentability—the essence of hindsight." *Ecolochem, Inc. v. So. Cal. Edison Co.*, 227 F.3d 1361, 1371-72 (Fed. Cir. 2000) (quoting *In re Dembiczak*, 175 F.3d 994, 999 (Fed. Cir. 1999)).

Applicants submit that the current construction of the cited references in the manner provided in the Office Action requires hindsight reasoning, which the Federal Circuit has explicitly rejected. *See In re Fritch*, 972 F.2d 1260, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992). As stated above, *Sriram* does not teach the limitations as recited in claims 1 and 8. Neither *Yin*, nor *Weng* correct these failings of *Sriram*. It would not have been obvious to one of ordinary

skill in the art to combine *Sriram* and *Yin* or *Weng*, and the subject matter of the limitations **not** taught by said references, to arrive at the presently claimed invention. A motivation to combine *Sriram* and *Yin* merely creates *Sriram* plus an unnecessary communication link and *Sriram* and *Weng* merely creates *Sriram* plus a buffer size based on maximum packet length. To conclude that such a combination provides the presently claimed invention requires hindsight reasoning. Applicants earnestly request reconsideration, withdrawal of this rejection, and allowance of claims 1-14.

IV. Conclusion

Claims 1-14 are currently pending in the patent application. Of these pending claims, only claims 1 and 8 are independent claims. Since the Applicants respectfully assert that these independent claims are allowable, dependent claims 2-7 and 9-14 are also allowable.

Sriram does not anticipate any of the pending claims. *Sriram*, in combination with *Yin* does not render obvious any of the pending claims, as the references fail to teach or suggest all the claim limitations and to combine *Sriram*, *Yin*, and the limitations of the claims not taught by either requires hindsight reasoning. *Sriram*, in combination with *Weng* does not render obvious any of the pending claims, as the references fail to teach or suggest all the claim limitations and to combine *Sriram*, *Weng*, and the limitations of the claims not taught by either requires hindsight reasoning. Hence, claims 1-14 are in a condition for allowance.

In light of the remarks above, the Applicants respectfully request that the Examiner send the application to issuance. If the Examiner believes that a telephone conference will facilitate an expeditious issuance of the current Application, the Examiner is invited to call the undersigned attorney.

Under 37 C.F.R. §1.114, a Request for Continued Examination must be accompanied with a submission. This reply satisfies the requirement of a submission because it is fully responsive.

A fee of $810.00 for a request for continued examination fee is enclosed. The Commissioner is hereby authorized to apply this fee and any additional fees which may be required, or credit any overpayment to Deposit Account No. 14-0629.

Respectfully submitted,

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